Section 7

Rigid Disk Preamplifiers and Servo Control Circuits

7

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DP117-X/DP117-XR/μA117-X/μA117-XR Series Winchester Disk Read/Write Preamplifiers

General Description

The DP117-X/DP117-XR, μA117-X/μA117-XR Series High Performance Read/Write Preamplifiers are intended for use in Winchester disk drives which employ center tapped ferrite or manganese-zinc read/write heads. The circuit can interface with up to eight read/write heads which makes it ideal for multi-platter disk drive designs. Designed to reside in the Head/Disk Assembly (HDA) of Winchester disk drives, the Read/Write Preamplifiers provide termination, gain, and output buffering for the disk heads as well as switched write current. Certain write fault conditions are detected and reported to protect recording integrity. The parts are available with internal damping resistor (DP117-R) and without internal damping resistor (DP117).

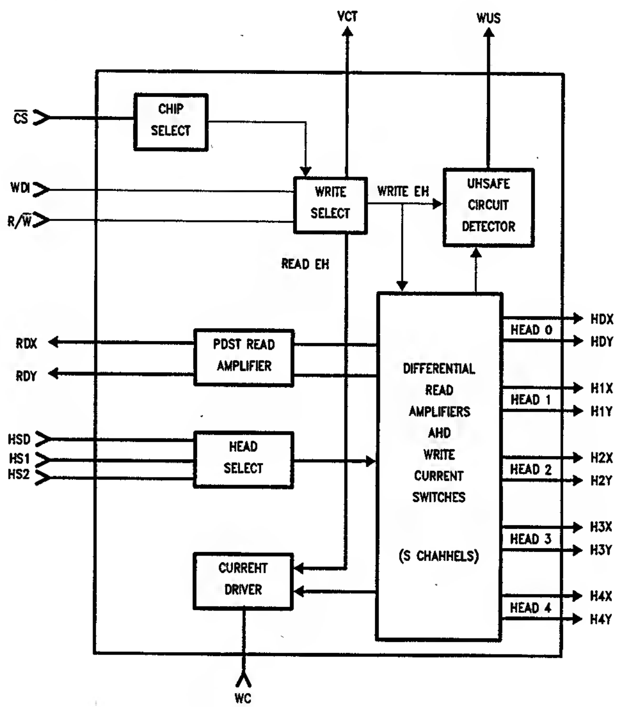
Features

- Wide bandwidth, high gain, low noise
- Up to eight read/write channels
- Internal write fault condition detection
- 5.0V and 12V power supply voltages
- Independent read and write data lines
- TTL control and data logic levels
- Externally programmable write current
- Available with internal damping resistor
- Compatible with SSI 117 family

Part Selection

Device Code	Channels
μA117-2	2
μA117-4	4
μA117-6	6

Block Diagram (Typical, DP117-X)



TL/F/9406-7

Absolute Maximum Ratings All voltages referenced to GND

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic	−65°C to +175°C
Plastic	−65°C to +150°C
Operating Junction Temperature Range	+25°C to +135°C
Lead Temperature	
Ceramic (Soldering, 60 seconds)	300°C
Plastic (Soldering, 10 seconds)	265°C
Internal Power Dissipation (Notes 1 & 2)	
28L-Ceramic DIP	2.50W
24L-Ceramic DIP	1.95W
18L-Ceramic DIP	1.58W
24L-Brazed Flatpak	0.97W
24L-Ceramic Flatpak	0.90W
28L-PLCC	1.39W
Supply Voltage (V_{CC1})	6.0V
Supply Voltage (V_{CC2})	15V
Write Current (IWC)	70 mA
Input Voltage Range	
Head Select (HS0, HS1, HS2)	−0.4V to V_{CC1} + 0.3V
Write Current (WC) Voltage in read and idle modes. (Write mode must be current limited to −70 mA)	−0.3V to V_{CC1} + 0.3V
Chip Select (CS)	−0.4V to V_{CC1} + 0.3V
Read/Write (R/W)	−0.4V to V_{CC1} + 0.3V
DC Supply Voltage	
(V_{DD1})	−0.3V to +14V
(V_{DD2})	−0.3V to +14V
(V_{CC})	−0.3V to +6.0V
Digital Input Voltage Range (V_{IN})	−0.3V to V_{CC} + 0.3V
Head Port Voltage Range (V_H)	−0.3V to V_{DD} + 0.3V
WUS Port Voltage Range (V_{WUS})	−0.3V to +14V
Write Current (I_W)	60 mA
Output Current (I_O)	
RDX, RDY	−10 mA
VCT	−60 mA
WUS	+12 mA

Recommended Operating Conditions

DC Supply Voltage	
(V_{DD1})	12V ±10%
(V_{DD2})	6.5V to V_{DD1}
(V_{CC})	5.0V ±10%
Head Inductance (Lh)	5.0 μH to 15 μH
Damping Resistor (External) (RD)	500Ω to 2000Ω
RCT Resistor (RCT)	90Ω ±5.05 (½W)
Write Current (I_W)	25 mA to 50 mA
RDX, RDY Output Current (I_O)	0 μA to 100 μA

Note 1: $T_{J\,MAX}$ = 150°C for the Plastic, and 175°C for the Ceramic.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 26L-Ceramic DIP at 16.7 mW/°C, the 24L-Ceramic DIP at 13 mW/°C, the 18L-Ceramic DIP at 10.5 mW/°C, the 24L-Brazed Flatpak at 6.5 mW/°C, the 24L-Ceramic Flatpak at 6.0 mW/°C, and the 26L-PLCC at 11.2 mW/°C.

DC Characteristics $25°C \le T_J < 125°C$, V_{DD1} = 12V, V_{CC} = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current	Read/Idle Mode			25	mA
		Write Mode			30	
I_{DD}	Supply Current	Idle Mode			25	mA
		Read Mode			50	
		Write Mode			30 + I_W	
P_C	Power Consumption	T_J = 125°C	Idle Mode		400	mW
			Read Mode		600	
			Write Mode, I_W = 50 mA RCT = 90Ω RCT = 0Ω		850 1050	
V_{IL}	Digital Inputs: Input Voltage LOW			−0.3	0.8	V
V_{IH}	Digital Inputs: Input Voltage HIGH			2.0	V_{CC} + 0.3	V
I_{IL}	Digital Inputs: Input Current LOW	V_{IL} = 0.8V		−0.4		mA
I_{IH}	Digital Inputs: Input Current HIGH	V_{IH} = 2.0V			100	μA
V_{OL}	WUS Output	I_{OL} = 8.0 mA			0.5	V
I_{OH}		V_{OH} = 5.0V			100	μA
V_{CT}	Center Tap Voltage	Read Mode		4.0 (typ)		V
		Write Mode		6.0 (typ)		V

Write Characteristics V_{DD1} = 12V, V_{CC} = 5.0V, I_W = 45 mA, Lh = 10 μH, f (Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, $R_{D\ EXT}$ = 750Ω or $R_{D\ INT}$, unless otherwise specified

Parameter	Conditions	Min	Max	Units
Write Current Range		10	50	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7		V (pk)
Unselected Differential Head Current			2.0	mA (pk)
Differential Output Capacitance			15	pF
Differential Output Resistance	Without Internal Resistors	10k		Ω
	With Internal Resistors	538	1.0k	
WDI Transition Frequency	WUS = LOW	400 (typ)		kHz
I_{WC} to Head Current Gain		18 (typ)		mA/mA

Read Characteristics V_{DD1} = 12V, V_{CC} = 5.0V, Lh = 10 μH, f (Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, (V_{in} is referenced to V_{CT}), $R_{D\ EXT}$ = 750Ω or $R_{D\ INT}$, unless otherwise specified

Parameter	Conditions		Min	Max	Unit
Differential Voltage Gain	V_{IN} = 1.0 mV_{p-p} at 300 kHz RL (RDX), RL (RDY) = 1.0 kΩ		80	120	V/V
Dynamic Range	Input Voltage, V_I, where gain falls by 10%. V_{IN} = V_I + 0.5 mV_{p-p} at 300 kHz		−2.0	2.0	mV
Bandwidth (−3 dB)	I Zs I < 5.0Ω, V_{IN} = 1.0 mV_{p-p}		30		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			2.1	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5.0 MHz			23	pF
Differential Input Resistance	f = 5.0 MHz	Without Internal Resistors	2k		Ω
		With Internal Resistors	440	850	
Input Bias Current				45	μA
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100 mV_{p-p} at 5.0 MHz		50		dB
Power Supply Rejection Ratio	100 mV_{p-p} at 5.0 MHz on V_{DD1}, V_{DD2} or V_{CC}		45		dB
Channel Separation	Unselected Channels: V_{IN} = 100 mV_{p-p} at 5.0 MHz and Selected Channel: V_{IN} = 0 mV_{p-p}		45		dB
Output Offset Voltage			−480	480	mV
Common Mode Output Voltage			5.0	7.0	V
Single Ended Output Resistance	f = 5.0 MHz			35	Ω
Internal Damping Resistor			560	1070	Ω

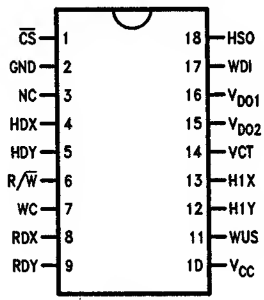
Switching Characteristics

V_{DD1} = 12V, V_{CC} = 5.0V, T_J = 25°C, I_W = 45 mA, Lh = 10 μH, f (Data) = 5.0 MHz, $R_{D\ EXT}$ = 750Ω or $R_{D\ INT}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
R/$\overline{W}$	R/$\overline{W}$ to Write	Delay to 90% of Write Current		1.0	μs
	R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% Decay of Write Current		1.0	
$\overline{CS}$	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope		1.0	μs
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		1.0	
HS0 HS1 HS2	to Any Head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope		1.0	μs
WUS	Safe to Unsafe—TD1	I_W = 50 mA	1.6	8.0	μs
	Unsafe to Safe—TD2	I_W = 20 mA		1.0	
Head Current	Propagation Delay—TD3, TD4	Lh = 0 μH, Rh = 0Ω from 50% Points		25	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time		2	
	Rise/Fall Time	10%–90% Points		20	

Connection Diagrams

18-Lead Molded DIP



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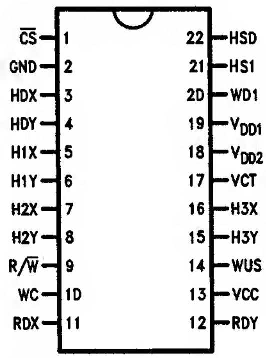
Top View

†Order Number μA1172DC or μA1172RDC
††See NS Package Number N18A

22-Lead Molded DIP



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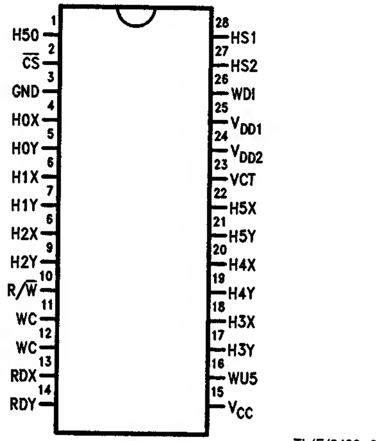
Top View

†Order Number μA1174PC or μA1174RPC
††See NS Package Number N22A

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Connection Diagrams (Continued)

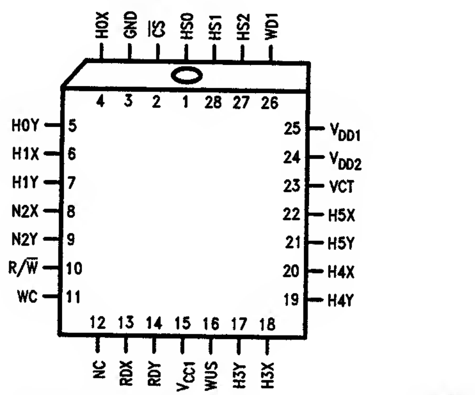
28-Lead DIP



Top View

†Order Number μA1176PC or μA1176RPC
††See NS Package Number N28B

28-Lead PLCC



Top View

†Order Number μA1176QC or μA1176RQC
††See NS Package Number V28A

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Functional Description

In the Write mode, the DP117-X/DP117-XR, μA117-X/μA117-XR Series accepts TTL compatible write data pulses on the WDI lead. On the falling edge of each write data pulse, a current transition is made in the selected head. Head selection is accomplished via TTL input signals: HS0, HS1, HS2 (see Table II). Internal circuitry senses the following conditions:

1. Absence of data transitions.
2. Open circuit head connection.
3. Absence of write current.
4. Short circuit head connection.
5. Idle or read mode.

Any or all of the above conditions would result in a high level on the write unsafe (WUS) output signal.

During read operations, the DP117-X amplifies the differential voltages appearing across the selected R/W head lead and applies the amplified signal differentially to data lines RDX and RDY.

Pin Descriptions

Lead	Name	Function
$\overline{CS}$	Chip Select	Chip Select High disables the read/write function of the device and forces idle mode. (TTL)
R/$\overline{W}$	Read/Write Select	A Logic High places the devices in read mode and a Logic Low forces write mode. Refer to Table I. (TTL)
H0X, Y through H5X, Y	Read/Write Head Connections	The DP117 has five pairs of read/write connections. The X and Y phases are made consistent with the read output, RDX and RDY, phases. (Differential)
RDX, Y	Read Data Outputs	The chip has one pair of read data outputs which is multiplexed to the appropriate head connections. (Differential)
HS0 through HS2	Head Select Inputs	The eight read/write heads are addressed with the head select inputs. Refer to Table II. (TTL)
WC	Write Current Input	This lead sets the current level for the write mode. An external resistor is connected from this lead to ground, and write current is determined by the value of this resistor divided into the write current constant K, which is typically 140V.
WDI	Write Data Input	The write data input toggles the write current between the X and Y selected head connections. Write current is switched on the negative edge of WDI. The initial direction for write current is the X side of the switch and is set upon entering read or idle mode. (TTL)
V_{DD2}	Resistor Center Tap	In some versions (determined by lead availability) of the DP117-X series, a resistor may be connected between RCT and V_{DD1} to reduce internal power dissipation. If this resistor is not used, RCT must be connected externally to V_{DD1}.
VCT	Center Tap Voltage	The center tap output provides bias voltage for the head inputs in read and write mode. It should be connected to the center tap of the read/write heads.
WUS	Write Unsafe	A high logic level at the write unsafe output indicates a fault condition during write. Write unsafe will also be high during read and idle mode. (Open collector)

TABLE I. Read/Write Select

Operating Modes		
Chip Select $\overline{CS}$	Read/Write R/$\overline{W}$	Mode
1	X	Idle
0	1	Read
0	0	Write

TABLE II. Head Select Inputs

Head Selection			
HS0	HS1	HS2	Head Selected (Note 1)
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5

Note 1: If selected head is beyond the capacity of the DP117-X model, the open input condition on the selected input will be reported as an unsafe level at the WUS output.

Timing Diagrams

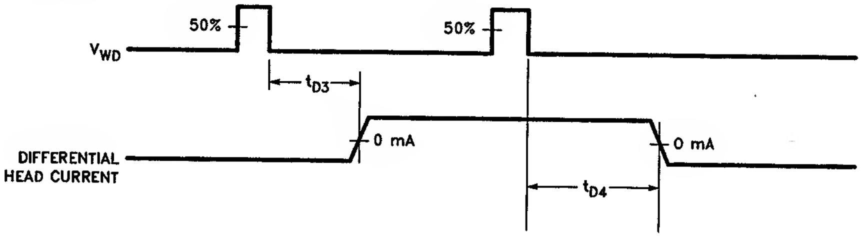


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FIGURE 1. Head Current Timing

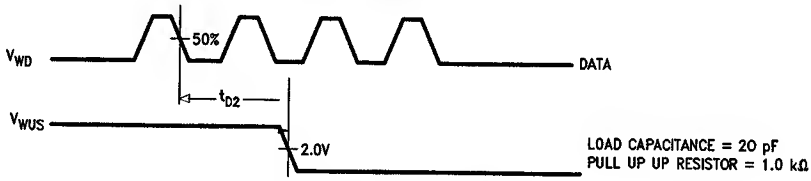

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FIGURE 2a. Unsafe to Safe Timing

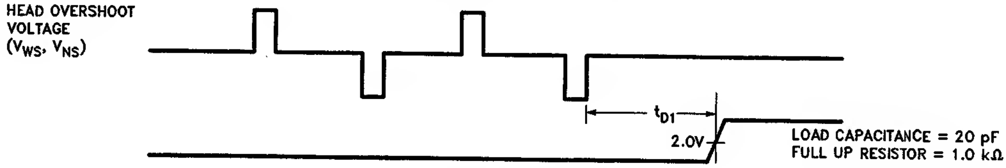

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FIGURE 2b. Safe to Unsafe Timing

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DP501X/DP501XR/μA501X/μA501XR Series 6 or 8 Channel Read/Write Circuit

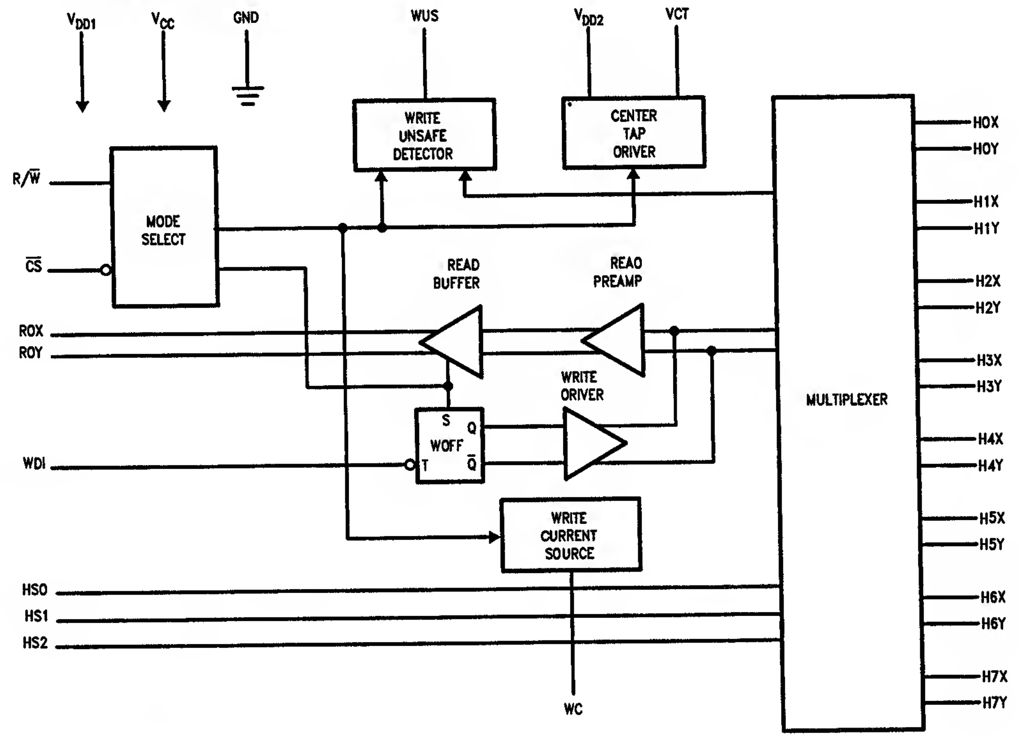
General Description

The μA501X/μA501XR devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for eight channels. The μA501X/μA501XR requires +5.0V and +12V power supplies and is available in a variety of packages. The μA501XR differs from the μA501X by having internal damping resistors.

Features

- +5.0V, +12V power supplies
- Single- or multi-platter Winchester drives
- Designed for center-tapped ferrite heads
- Programmable write current source
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals

Block Diagram



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Note: Caution: Use handling procedures necessary for a static sensitive component.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP and Flatpak	−65°C to +175°C
Molded DIP and PLCC	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP and Flatpak (Soldering, 60 seconds)	300°C
Molded DIP and PLCC (Soldering, 10 seconds)	265°C
Internal Power Dissipation (Notes 2 & 3)	
28L-Ceramic DIP	2.50W
28L-Plastic DIP	1.92W
32L-Brazed Flatpak	1.88W
40L-Ceramic DIP	2.65W
40L-Plastic DIP	2.5W
28L-Plastic LCC	1.39W
44L-Plastic LCC	1.92W
DC Supply Voltage	
V_{DD1} and V_{DD2}	−0.3V to +14V
V_{CC}	−0.3V to +6.0V
Digital Input Voltage Range	−0.3V to V_{CC} + 0.3V
Head Port Voltage Range	−0.3V to V_{DD} + 0.3V
WUS Port Voltage Range	−0.3V to +14V
1 Write Current	60 mA
Output Current	
RDX and RDY	−10 mA
VCT	−60 mA
WUS	+12 mA

Note 1: All voltages referenced to GND.

Note 2: $T_{J\,MAX}$ = 150°C for the Plastic, and 175°C for the Ceramic.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 18.7 mW/°C, the 28L-Plastic DIP at 15.3 mW/°C, the 32L-Brazed Flatpak at 12.5 mW/°C, the 40L-Ceramic DIP at 20.1 mW/°C, the 40L-Plastic DIP at 20 mW/°C, the 28L-Plastic LCC at 11.2 mW/°C, and the 44L-Plastic LCC at 15.3 mW/°C.

Recommended Operating Conditions

DC Supply Voltage	
V_{DD1}	12V ±10%
V_{CC}	5V ±10%
Head Inductance (Lh)	5.0 μH to 15 μH
Damping Resistor (External)	
RD (DP501X Only)	500Ω to 2000Ω
RCT Resistor	90Ω ±5.0% (½W)
Write Current (I_W)	25 mA to 50 mA

DC Electrical Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ +70°C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current	Read/Idle Mode		25	mA
		Write Mode		25	
I_{DD}	Supply Current	Idle Mode		20	mA
		Read Mode		40	
		Write Mode		20 + I_W	
P_C	Power Consumption	25°C ≤ T_J ≤ 135°C, Idle Mode		400	mW
		25°C ≤ T_J ≤ 135°C, Read Mode		650	
		25°C ≤ T_J ≤ 135°C, Write Mode, I_W = 50 mA, RCT = 90Ω		880	
		25°C ≤ T_J ≤ 135°C, Write Mode, I_W = 50 mA, RCT = 0Ω		1060	
V_{IL}	Digital Inputs: Input Voltage LOW		−0.3	0.8	V
V_{IH}	Digital Inputs: Input Voltage HIGH		2.0	V_{CC} + 0.3	V
I_{IL}	Digital Inputs: Input Current LOW	V_{IL} = 0.8V	−0.4		mA
I_{IH}	Digital Inputs: Input Current HIGH	V_{IH} = 2.0V		100	μA
V_{OL}	WUS Output	I_{OL} = 8.0 mA		0.5	V
I_{OH}		V_{OH} = 5.0V		100	μA
V_{CT}	Center Tap Voltage	Read Mode	4.0 (typ)		V
		Write Mode	6.0 (typ)		V

Write Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ +70°C, I_W = 45 mA, Lh = 10 μH, Rd = 750Ω (DP501X only), f(Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, unless otherwise specified

Parameter	Conditions	Min	Max	Units
Write Current Range		10	50	mA
Write Current Constant "K"		129	151	V
Differential Head Voltage Swing		7.5		V (pk)
Unselected Head Transient Current	5.0 μH ≤ Lh ≤ 9.5 μH		2.0	mA (pk)
Differential Output Capacitance			15	pF
Differential Output Resistance	Without Internal Resistors	10k		Ω
	With Internal Resistors	560	940	
WDI Transition Frequency	WUS = LOW	250		kHz
Head Current Gain to I_{WC} $\left(\frac{I_W}{I_{WC}}\right)$		20 (typ)		mA/mA
Unselected Head Leakage	Sum of X and Y Side Current		85	μA

Read Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, I_W = 45 mA, CL (RDX, RDY) ≤ 20 pF, (V_{IN} is referenced to V_{CT}), 0°C ≤ T_A ≤ + 70°C, Lh = 10 μH, Rd = 750Ω, f(Data) = 5.0 MHz unless otherwise specified

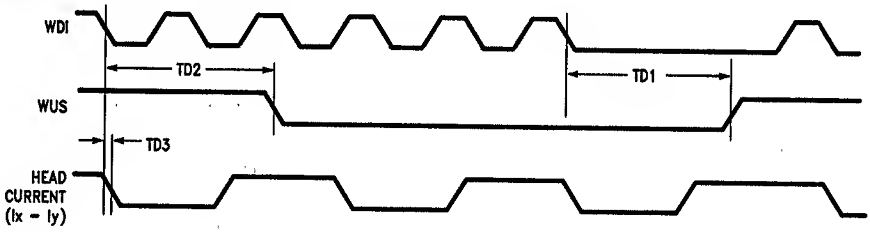
Characteristic	Condition		Min	Max	Unit
Differential Voltage Gain	V_{IN} = 1.0 mV_{PP} at 300 kHz RL (RDX), RL (RDY) = 1.0 kΩ (AC coupled)		80	120	V/V
Dynamic Range	Input Voltage, V_I, where Gain Falls by 10% V_{IN} = V_I + 0.5 mV_{PP} at 300 kHz		−3.0	3.0	mV
Bandwidth (−3 dB)	|Zs| < 5.0Ω, V_{IN} = 1.0 mV_{PP}		30		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5.0 MHz			23	pF
Differential Input Resistance	f = 5.0 MHz, V_{IN} ≤ 6 mV_{PP}	Without Internal Resistors	2k		Ω
		With Internal Resistors	530	790	
Input Bias Current (per Side)				100	μA
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100 mV_{PP} at 5.0 MHz		50		dB
Power Supply Rejection Ratio	100 mV_{PP} at 5.0 MHz on V_{DD1}, V_{DD2}, or V_{CC}		45		dB
Channel Separation	Unselected Channels: V_{IN} = 100 mV_{PP} at 5.0 MHz and Selected Channel: V_{IN} = 0 mV_{PP}		45		dB
Output Offset Voltage			−480	480	mV
Common Mode Output Voltage		Read Mode	5.0	7.0	V
		Write/Idle Mode	4.3 (typ)		
Single Ended Output Resistance	f = 5.0 MHz			30	Ω
External Resistive Load (AC Coupled to Output)	Per Side to GND		100		Ω
Leakage Current (RDX, RDY)	5.0 < RDX, RDY < 8.0V Write or Idle Mode		−50	50	μA
Center Tap Output Impedance	0 ≤ f ≤ 5.0 MHz			150	Ω
Output Current	AC Coupled Load RDX to RDY		2.0		mA

Switching Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ +70°C, I_W = 45 mA, Lh = 10 μH, Rd = 750Ω, f(Data) = 5.0 MHz, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
R/$\overline{W}$	R/$\overline{W}$ to Write	Delay to 90% of Write Current		600	ns
	R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% Decay of Write Current		600	
$\overline{CS}$	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope		600	ns
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		600	
HS0 HS1 HS2	to Any Head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope		600	ns
WUS	Safe to Unsafe—TD1	I_W = 50 mA	1.6	8.0	μs
	Unsafe to Safe—TD2	I_W = 20 mA		1.0	
Head Current	Propagation Delay—TD3	Lh = 0 μH, Rh = 0Ω from 50% Points		30	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time		2	
	Rise/Fall Time	10%–90% Points		20	

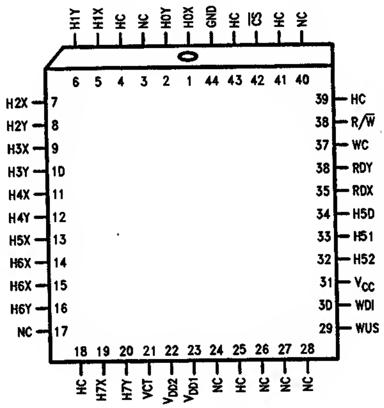
Write Mode Timing Diagram



TL/F/9407-8

Connection Diagrams

44-Lead PLCC

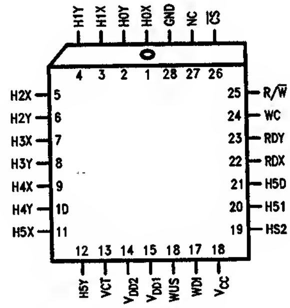


TL/F/9407-2

Top View

Order Number μA5018QC or μA5018RQC
See NS Package Number V44A

28-Lead PLCC

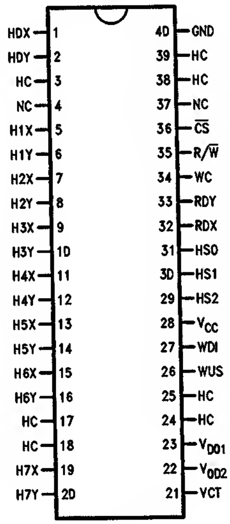


TL/F/9407-3

Top View

Order Number μA5016QC or μA5016RQC
See NS Package Number V28A

40-Lead DIP



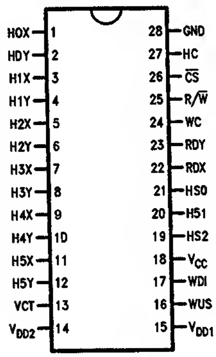
TL/F/9407-1

Top View

Ceramic DIP
***Order Number μA5018DC or μA5018RDC**
****See NS Package Number J40A**

Molded DIP
***Order Number μA5018PC or μA5018RPC**
****See NS Package Number N40A**

28-Lead DIP



TL/F/9407-5

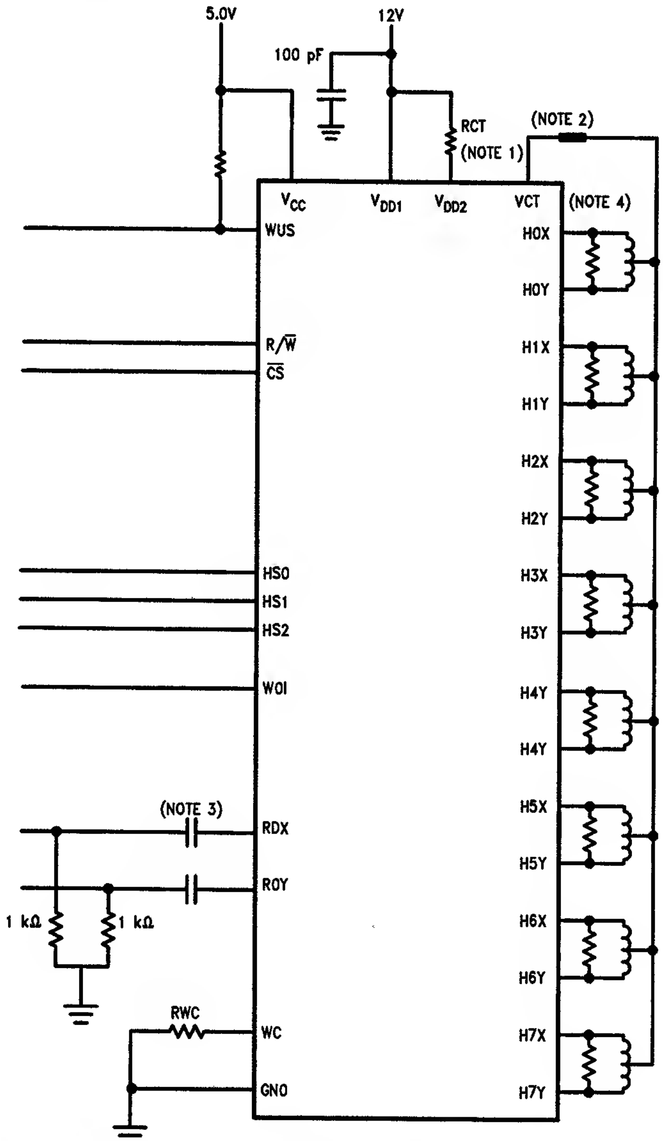
Top View

Order Number μA5016DC or μA5016RDC
See NS Package Number J28A

Order Number μA5016PC or μA5016RPC
See NS Package Number N28B

*For most current order information, contact your local sales office.
**For current package information, contact product marketing.

Application Information



TL/F/9407-7

Note 1: An external ½W resistor, RCT, given by RCT = 90 (50/I_W)Ω, where i_W is in mA can be used to limit internal power dissipetion. Otherwise connect V_{DD2} to V_{DD1}.

Note 2: A ferrite beed (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics.

Note 3: Limit DC current from RDX and RDY to 100 μA and load capacitance to 20 pF.

Note 4: Demping resistors required on DP501X oniy.

Pin Descriptions

TABLE I. Description of Lead Functions

Name	Functions
HS0–HS2	Head Select
$\overline{CS}$	Chip Select: a low level enables device.
R/$\overline{W}$	Read/Write: a high level selects read mode.
WUS	Write Unsafe: a high level indicates an unsafe writing position.
WDI	Write Data In: a negative transition toggles the direction of the head current.
H0X–H7X H0Y–H7Y	X, Y Head Connections
RDX, RDY	X,Y Read Data: differential read signal out.
WC	Write Current: used to set the magnitude of the write current.
VCT	Voltage Center Tap: voltage source for head center tap.
V_{CC}	+5.0V
V_{DD1}	+12V
V_{DD2}	Positive power supply for the center tap voltage source.
GND	Ground

Circuit Operation

The μA510X/μA501XR functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables II and III. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the μA510X/μA501XR as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

$$I_W = K/Rwc, \text{ where } K = \text{Write Current Constant}$$

is set by the external resistor, Rwc, connected from lead WC to GND.

TABLE II. Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	X	Idle

TABLE III. Head Select

HS2	HS1	HS0	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low Level
1 = High Level

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

READ MODE

In the Read mode the μA510X/μA501XR is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode. This eliminates the need for external gating of the write current source.

National Semiconductor

DP24H80/μA24H80 Winchester Disk Servo Preamplifier

General Description

The DP24H80/μA24H80 provides termination, gain, and impedance buffering for the servo read head in Winchester disk drives. It is a differential input, differential output design with fixed gain of approximately 100. The bandwidth is guaranteed greater than 30 MHz.

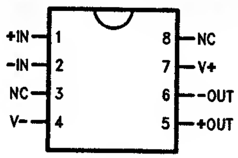
The internal design of the DP24H80/μA24H80 is optimized for low input noise voltage to allow its use in low input signal level applications. It is offered in 8-lead DIP, 10-lead flatpak, or SO-8 package suitable for surface mounting.

Features

- Low input noise voltage
- Wide power supply range (8V to 13V)
- Internal damping resistors (1.3 kΩ)
- Direct replacement for SSI 101A, with improved performance

Connection Diagrams

8-Lead DIP and SO-8 Package



TL/F/9408–1

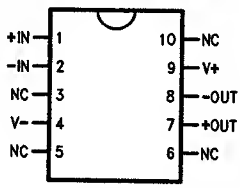
Top View

Ceramic DIP
† Order Number μA24H80RC
‡ See NS Package Number J08A

Molded Surface Mount
† Order Number μA24H80SC
‡ See NS Package Number M08A

Molded DIP
† Order Number μA24H80TC
‡ See NS Package Number N08E

10-Lead Ceramic Flatpak



TL/F/9408–2

Top View

† Order Number μA24H80FC
‡ See NS Package Number F10B

Pin Descriptions

Name	Description of Functions
V+	Positive Differential Supply with Respect to V−
V−	Negative Differential Supply with Respect to V+
+IN	Positive Differential Input
−IN	Negative Differential Input
+OUT	Positive Differential Output
−OUT	Negative Differential Output
NC	No Connection

† For most current order information, contact your local sales office.
‡ For current package information, contact product marketing.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP and Flatpak	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP and Flatpak (Soldering, 60 seconds)	300 °C
Molded DIP and SO-8 (Soldering, 10 seconds)	265°C
Internal Power Dissipation (Notes 1 & 2)	
8L-Ceramic DIP	1.30W
8L-Molded DIP	0.93W
SO-8	0.81W
10L-Flatpak	0.79W
Supply Voltage	15V
Output Voltage	15V
Differential Input Voltage	±10V

Note 1: $T_{J\ MAX}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Ceramic DIP and Flatpak.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, the SO-8 at 6.5 mW/°C, and the Flatpak at 5.3 mW/°C.

Electrical Characteristics T_A = 25°C, V_{CC} = 8V to 13.2V, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G	Gain (Differential) (Note 4)	R_p = 130Ω, V_{CC} = 12V	80	100	120	
		R_p = 130Ω, V_{CC} = 12V, T_A = 0°C to +70°C	70		130	
BW	Bandwidth (3.0 dB) (Note 2)	V_I = 0.5 $mV_{p\text{-}p}$	30	65		MHz
R_I	Input Resistance		1040	1300	1560	Ω
C_I	Input Capacitance			3		pF
V_I	Input Dynamic Range (Differential)	R_p = 130Ω, V_{CC} = 12V	3			$mV_{p\text{-}p}$
I_S	Supply Current	V_{CC} = 12V		20	25	mA
ΔV_O	Output Offset (Differential)	R_p = 130Ω, R_s = 0Ω			200	mW
V_n	Equivalent Input Noise (Notes 2 & 3)	R_s = 0Ω, BW = 4 MHz		1.5	2	μV
PSRR	Power Supply Rejection Ratio (Note 1)	R_s = 0Ω, f = 5 MHz	55	70		dB
ΔG/ΔV	Gain Sensitivity (Supply)	R_p = 130Ω, ΔV_{CC} = ±10%			±0.5	%/V
ΔG/ΔT	Gain Sensitivity (Temp)	R_p = 130Ω, T_A = 25°C to +70°C		−0.1		%/°C
CMR	Common Mode Rejection (Note 1) (Input)	f = 5 MHz	60	75		dB

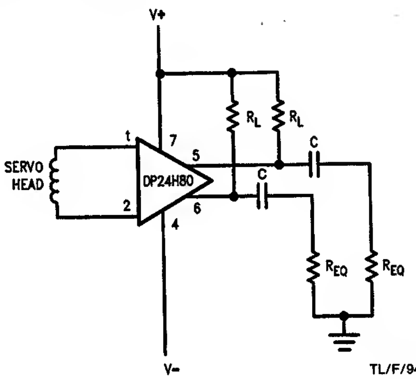
Note 1: Tested at DC, guaranteed at frequency.

Note 2: Guaranteed, but not tested in production.

Note 3: Equivalent input noise (additional specification):

Typ	Max	Unit	Condition
3	4	μV	BW = 15 MHz2
0.85	1.0	nV/√Hz	BW = 15 MHz2

Typical Applications



TL/F/9408-3

Note 1: Leads shown for 8-lead DIP.

Note 2: R_{eq} is equivalent load resistance.

Note 3: $R_p = \dfrac{R_L \bullet R_{eq}}{R_L + R_{eq}}$

Note 4: G = 0.77 R_p
Where R_p = value from Note 3 (above) in ohms.

National Semiconductor

DP2580/μA2580
Winchester Disk Servo Preamplifier

General Description

The DP2580 provides termination, gain, and impedance buffering for the thin film servo read head in Winchester disk drives. It is a differential output design with fixed gain of approximately 250. The bandwidth is guaranteed greater than 30 MHz.

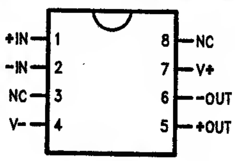
The internal design of the DP2580 is optimized for low input noise voltage to allow its use in low input signal level applications. It is offered in 8-lead ceramic DIP, 10-lead Flatpak, and an SO-8 package suitable for surface mounting.

Features

- Low input noise voltage — Typ. 0.5 nV/$\sqrt{Hz}$
- Wide power supply range — 8V to 13V
- Internal damping resistors — 1 kΩ

Connection Diagrams

8-Lead DIP and SO-8 Package



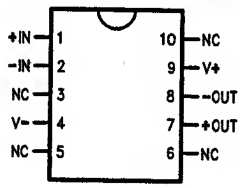
TL/F/9409-1

Top View

†Order Number μA2580DC
††See NS Package Number N08E

†Order Number μA2580SC
††See NS Package Number M08A

10-Lead Ceramic Flatpak



TL/F/9409-2

Top View

†Order Number μA2580FC
††See NS Package Number F10B

Pin Description

Name	Function
+IN	Positive Differential Input
−IN	Negative Differential Input
NC	No Connection
V−	Negative Differential Supply with Respect to V_{CC}
+OUT	Positive Differential Output
−OUT	Negative Differential Output
V+	Positive Differential Supply with Respect to V_{CC}
NC	No Connection

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP and Flatpak	−65°C to +175°C
SO-8	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP and Flatpak (Soldering, 60 seconds)	300°C
SO-8 (Soldering, 10 seconds)	265°C
Internal Power Dissipation (Notes 1 and 2)	
8L—Ceramic DIP	1.3W
10L—Flatpak	0.79W
SO-8	15V
Supply Voltage	15V
Output Voltage	15V
Differential Input Voltage	±1V

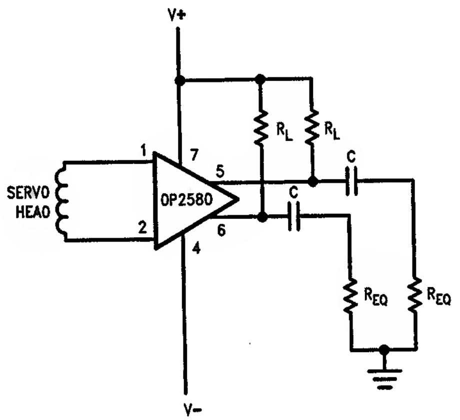
Note 1: T_J Max = 150°C for the SO-8, and 175°C for the Ceramic DIP and Flatpak.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L—Ceramic DIP at 8.7 mW/°C, the 10L—Flatpak at 5.3 mW/°C, and the SO-8 at 6.5 mW°C.

Electrical Characteristics T_A = 25°C, V+ − V− = 8V to 13.2V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G	Gain (Differential)	R_P = 100Ω, (V+) − (V−) = 12V		250		
BW	Bandwidth (3 dB)	V_I = 0.5 mV_{p-p}	30	65		MHz
R_I	Input Resistance			300		Ω
C_I	Input Capacitance			35		pF
V_I	Input Dynamic Range (Differential)	R_P = 100Ω, (V+) − (V−) = 12V			1	mV_{PP}
I_S	Supply Current	(V+) − (V−) = 12V		28	40	mA
ΔV_O	Output Offset (Differential)	R_s = 0Ω, R_P = 100Ω	600		600	mV
V_n	Equivalent Input Noise	BW = 4 MHz		0.6		nV/√Hz
PSRR	Power Supply Rejection Ratio	R_s = 0Ω, f = 5 MHz	50	65	0.90	dB
ΔG/V	Gain Sensitivity (Supply)	Δ (V+) − (V−) ±10%, R_P = 100Ω			0.5	%/V
ΔG/T	Gain Sensitivity (Temp.)	T_A = 25°C to 70°C, R_P = 100Ω		0.16		%/°C
CMR	Common Mode Rejection (Input)	f = 5 MHz	60	70		dB

Typical Applications (Notes 1–4)



TL/F/9409-3

Note 1: Leads shown for 8-lead DIP.

Note 2: R_{EQ} is equivalent load resistance.

Note 3: $R_P = \dfrac{R_L \bullet R_{EQ}}{R_L + R_{EQ}}$

Note 4: G = 2.5 R_P
Where R_P = value Note 3 (above) in Ω.

National Semiconductor

DP2460/DP2461, µA2460/µA2461 Servo Control Chips

General Description

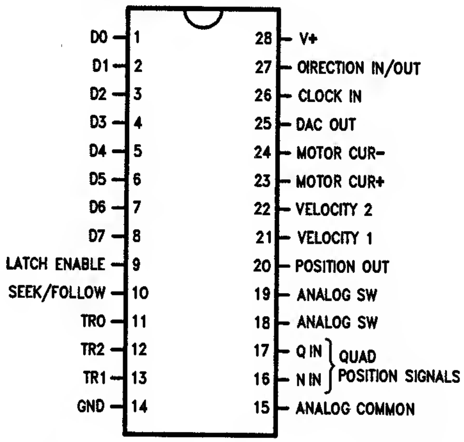
The DP2460 and DP2461 provide the analog signal processing required between a drive resident microprocessor and the servo power amplifier for Winchester disk closed loop head positioning. The DP2460 and DP2461 receive quadrature position signals from the servo channel; and from these, derive actual head seek velocity as well as position-mode off-track error. In the seek mode, the Digital to Analog Converter (DAC) is used to command velocity, while actual velocity is obtained by differentiating the quadrature position signals provided at V1 for external processing. The velocity signal (V2), obtained by integrating the motor current, is also available for extra damping, if desired. Further, the DAC may be used for detenting the head off-track for any purpose such as thermal compensation or soft-error retries.

Features

- Microprocessor compatible interface
- Quadrature di-bit compatible
- On board DAC
- Velocity V1 derived from position signal
- Velocity V2 derived from motor current
- Quarter-Track-Crossing signal outputs
- Minimal external components
- Compatible with DP2470 demodulator

Connection Diagrams

28-Lead Ceramic DIP

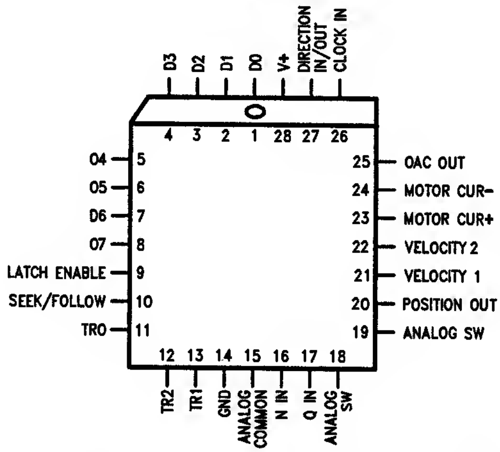


TL/F/9410-1

Top View

†Order Number µA2460DC or µA2461DC
††See NS Package Number J26A

26-Lead PLCC



TL/F/9410-2

Top View

†Order Number µA2460QC or µA2461QC
††See NS Package Number V26A

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
PLCC	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
PLCC (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Notes 1 and 2)	
28L—Ceramic DIP	2.50W
28L—PLCC	1.39W
Supply Voltage	15V Max
Analog Common Voltage	8.0V Max
All Inputs	V_{supply} Max

Note 1: T_J max = 150°C for the PLCC, and 175°C for the Ceremic DIP.

Note 2: Ratings apply to embient temperature et 25°C. Above this temperature, derate the 28L—Ceramic DIP at 16.7 mW/°C, end the 28L—PLCC et 11.2 mW/°C.

Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = 12V, f_{CLK} = 2.0 MHz, Analog Common = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital I/O	Input Voltage LOW				0.8	V
	Input Voltage HIGH		2.0			
	Output Voltage LOW	I_{OL} = 2.5 mA			0.45	
	Output Voltage HIGH	I_{OH} = 40 μA	2.4			
	Input Load Current	V_I = 0V to V_{CC}			0.2	mA
Clock Input	Input Comparator Reference Level		2.0	2.5	3.0	V
	Input Impedance		15	20		kΩ
DAC	Linearity (Note 1)		−1		1	LSB
	Resolution			8.0		bits
	Differential Nonlinearity		Monotonicity Guaranteed			
	Full Scale Output Voltage	Direction in High	7.25	7.35	7.45	V
		Direction in Low	2.55	2.65	2.75	
	Zero Scale Voltage			5.0		
	Output Offset Voltage				±10	mV
	Settling Time (Notes 2, 4)	To ½ LSB All bits ON or OFF				μs
Position Inputs	Input Voltage Range		1.0		9.0	V
	Input Impedance		15	20		kΩ
Analog Switch	On Resistance	V_{CM} = 0V to 12V		100	200	Ω
	Off Leakage (Note 3)			2.0	100	nA
Position Output	Output Voltage Swing	R_L = 15k Follow Mode	1.0		9.0	V
	Voltage Gain		0.9		1.1	—
	Output Offset Voltage				±20	mV
Velocity Outputs	Output Voltage Swing	R_L = 15k	1.0		9.0	V
	Output Offset Voltage V2				±20	mV
	Output Offset Voltage V1				15	
I_{CC}	Positive Supply	V_{CC} = 13.2V		10	15	mA
I_{SS}	Negative Supply	V_{CC} = 13.2V	−15	−10		mA
I_{AC}	Analog Common I		−2.0	0	2.0	mA
V1—Differentiator	Linearity	f_{CLK} = 1.0 MHz to 4.0 MHz; $f_{N/Q}$ ≤ 10 kHz		0.25		%
V2—Integrator	Linearity	f_{CLK} = 1.0 MHz to 4.0 MHz		1.0		%

Note 1: DAC Linearity is a function of the Clock frequency; Lineerity et 1.0 MHz is typically ±½ LSB.

Note 2: DAC Settling Time is approx. 5.0 μe, plus e delay of maximum 32 × Clock period i.e., 5 + 32 μs et Clock = 1.0 MHz Minimum could be 5.0 μs.

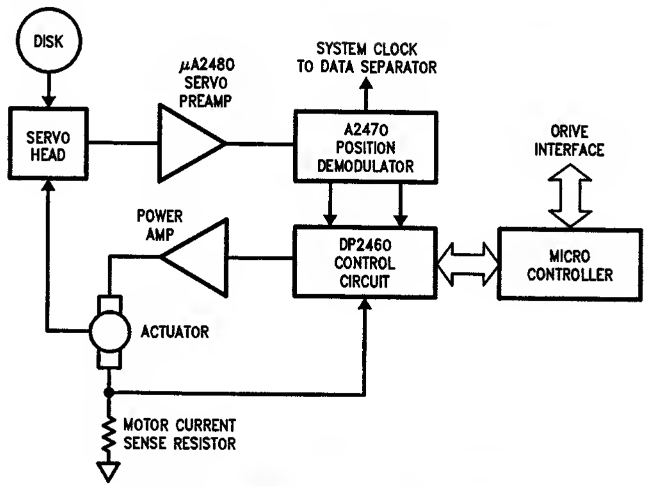
Note 3: Equivalent to 50 MΩ.

Note 4: Guaranteed, but not tested in production.

Pin Description

Pin No.	Name	Function
INPUTS		
1–8	DAC Input Word (D_0–D_7)	Programs DAC output, 00000000 = Analog Command Lead 1 = LSB Lead 8 = MSB
9	Latch Enable	Allows present DAC input word to be latched.
10	Seek/Follow Mode	Configures the feedback loop for either seeking or track-following. (High = Seek, Low = Follow)
14	Ground	
15	Analog Common	Analog signal reference input level (5.0V)
16	●	Normal position input signal.
17	Q	Quadrature position input signal.
23	Motor Current +	Motor current sense input to motor current integrator.
24	Motor Current −	
26	Clock	4.0 MHz (maximum) input square wave.
27	Direction In/Out	Changes the polarity of DAC output from positive to negative consistent with the desired direction of head motion.
28	V+	12V supply

Pin No.	Name	Function
OUTPUTS		
11	Track 2^0 (TR0)	TTL signal whose frequency is 8 times N (or Q).
12	Track 2^2 (TR2)	TTL signal indicating N > Q (for DP2460). TTL signal whose frequency is 2 times N (or Q) (for DP2461).
13	Track 2^1 (TR1)	TTL signal indicating $\overline{N}$ > Q (for DP2460). TTL signal whose frequency is 4 times N (or Q) (for DP2461).
18	Analog Switch	Analog switch to be used externally for changing from seek to follow.
19	Analog Switch	
20	Position Output	Analog signal representing sensed off track amplitude.
21	Velocity 1	Analog output representing velocity processed from position signals N and Q.
2●	Velocity 2	Analog output representing the integral of motor current.
25	DAC Output	Used to command velocity and position.



TL/F/9410–3

FIGURE 1. Head Actuator Control System

Functional Description

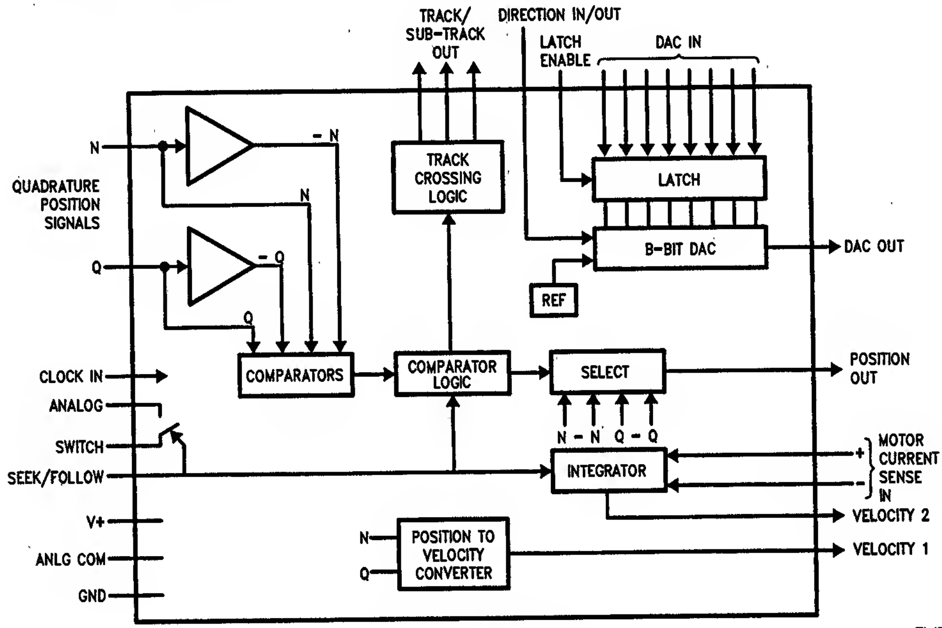


FIGURE 2. Block Diagram

Figure 2 shows a block diagram of the DP2460/DP2461 Servo Controller.

POWER SUPPLY AND REFERENCE REQUIREMENTS

The DP2460/DP2461 is designed to operate from a single supply of 10V to 12V. Also required is a reference voltage of 5.0V called Analog Common which serves two functions; all analog signals will be referenced to this voltage and in addition the internal DAC will use it to set full scale.

A clock signal must be provided as a reference for the internal switched capacitor position differentiator and motor current integrator. The clock signal should be a sine or square wave between Analog Common and ground at a maximum frequency of 4.0 MHz.

All digital inputs and outputs are TTL compatible levels referenced to ground.

INPUT SIGNALS AND TRACK CROSSING OUTPUTS

The input format selected for position feedback is consistent with a large class of sensors that generate two cyclical output signals displaced in space phase by 90 degrees (quadrature signal pairs). These sensors include resolvers, inducto-syns, optical encoders, and most importantly, servo demodulators designed for rigid disk head position sensing.

The input signals N and Q are quadrature quasi triangular waveforms with amplitudes of ±2.5V nominal referenced to Analog Common. The periods of the input signals are subdivided by internal comparators and logic and sent to the Track Crossing outputs T_0, T_1, and T_2. The relationship of these outputs to the inputs N and Q is shown in *Figure 3a* (for DP2460) and *Figure 3b* (for DP2461).

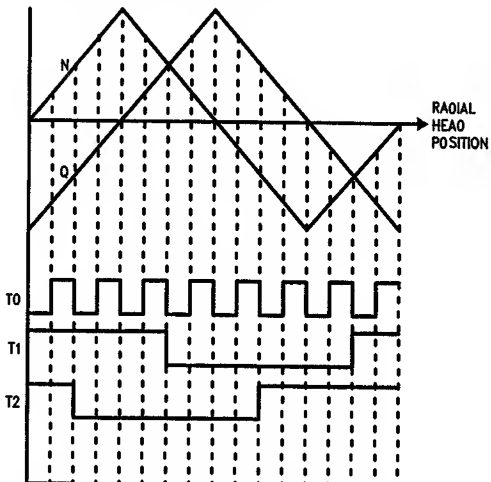
Note that different servo patterns may yield different numbers of track centerlines for each period of the quadrature signal pair. The relationship of T_0, T_1, and T_2 to N and Q is independent of track centerlines, leaving the correct interpretations to the microcontroller.

DAC

The DAC is an 8-bit, buffered input, voltage output digital to analog converter. The output voltage with an input code of all zeros is equal to Analog Common. Full scale is equal to Analog Common ±2.35V. The polarity depends on the Direction In Signal; Direction In High will result in a positive DAC output.

The DAC enable line when high will cause the DAC's input buffer to become transparent, i.e. input data will affect the output voltage immediately. When DAC enable is brought

Functional Description (Continued)



T0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1
T2	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1

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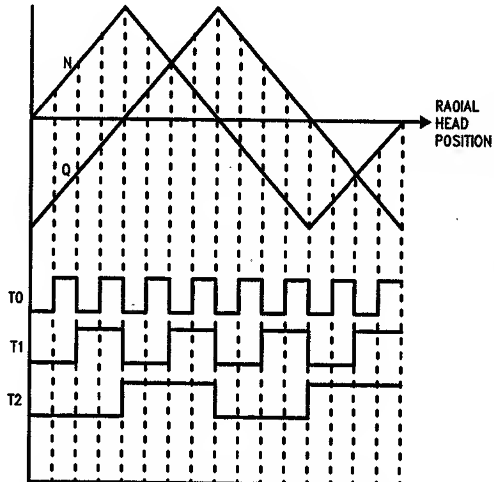
FIGURE 3a. Track Crossing Outputs (for DP2460)



T0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
T2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

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FIGURE 3b. Track Crossing Outputs (for DP2461)

low the data present on the input lines will be latched and any further changes to the input data will not change the output voltage. The DAC functions in both Seek and Follow Mode. During Seek Mode the DAC output is used as a velocity reference. In Follow Mode the DAC output can be summed into the position reference signal to offset the heads from track center.

ANALOG SWITCH

An uncommitted single pole single throw analog switch with an ON resistance of approximately 100Ω is provided. This switch is ON during Follow Mode.

MODE SELECT

The two major intended operating modes for the DP2460 are controlled by the microcontroller via the SEEK/FOLLOW input. Mode Select input high enables Seek Mode, low enables Track Follow Mode.

SEEK, when asserted by the microcontroller along with DIRECTION and a non-zero VELOCITY value as inputs, causes the actuator system to accelerate in the requested direction. During the ensuing motion, the actuator system will come under velocity feedback control. The velocity feedback signal is created by differentiation of the quadrature position signals and, additionally, by integration of motor current.

FOLLOW, the negation of SEEK, changes the feedback loop to a track-following or position mode. Position servos are typically second order systems and without loop compensation are potentially unstable. External components are used, along with the DP2460, to achieve stable track following performance. Velocity information (V1) is made available as an output in this mode to aid in stabilizing certain loops. If non-zero data is supplied to the velocity latches in this mode, it will result in a track offset in the direction indicated by DIRECTION IN/OUT. *Figure 4* shows typical seek operation.

POSITION OUTPUT

When the DP2460/DP2461 is set to Seek Mode the signal from Position Output lead is shown in *Figure 5*. This signal is made by switching the position inputs, (N and Q) through an inverter if required, ($\overline{N}$ and $\overline{Q}$) to the output using the track crossing signals. It can be used, if desired, to interpolate between DAC steps by attenuating it and summing it with the DAC output.

Track Follow Mode is entered when the heads are near the end of a seek, usually within one half to one track away from the target track centerline. The final setting to the track center is done by the position loop.

When the device is switched to Follow Mode, the position input signal (N, $\overline{N}$, Q or $\overline{Q}$) that is currently selected to the output is latched and the Position Out signal follows the selected position input signal until the device is switched back to Seek Mode. This implies that the switch to Follow Mode must not be made until the signal that will be the correct Position error signal for the target track is present at the output. If track centers are defined as the zero crossings of both N and Q this means that the switch to Follow Mode must be made less than one-half track away from the target track. (This is with respect to the convention of 4 tracks per encoder cycle, so switching must be done within 90° of the period of N or Q.)

Functional Description (Continued)

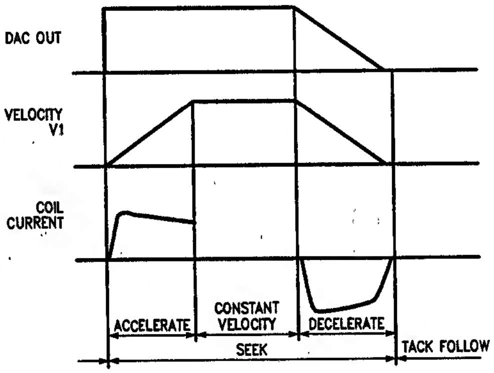


FIGURE 4. Typical Seek

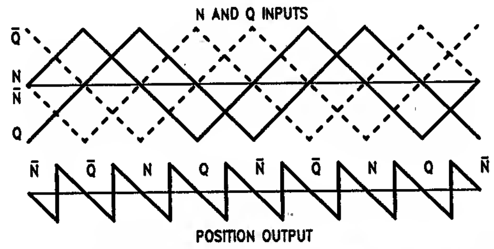


FIGURE 5. Position Output during Seek Mode

VELOCITY OUTPUTS

There are two analog signal outputs representing velocity. The first (V1) is derived by differentiating the position input signals. The entire differentiator is on-chip, using switched capacitor techniques and requires no external components.

The transfer function of the differentiator is:

$$V_O = dv/dt\,(\text{input}) \times 14.3/f\,(\text{clock})\ \text{Hz}$$

As an example; a 10 kHz triangular signal pair into N and Q of 6.0V peak-to-peak amplitude (dv/dt = 120 kV/s) would result in a velocity voltage output of 1.716V referenced to Analog Common with a clock of 1.0 MHz. The polarity will be positive if N is leading Q by 90 degrees and negative if Q is leading N. This block functions during both Seek and Follow modes.

The second velocity output is obtained by integrating a voltage proportional to the current in the motor using the following function:

$$dv/dt\,(\text{out}) = V\,(+I_{in} - -I_{in}) \times 2 \times 10^{-4}\,f\,(\text{clock})\ \text{Hz}.$$

The motor current integrator output is clamped to Analog Common during Follow Mode and is released at the initiation of a seek.

Figure 6 shows a typical application setup for the Servo Control chip.

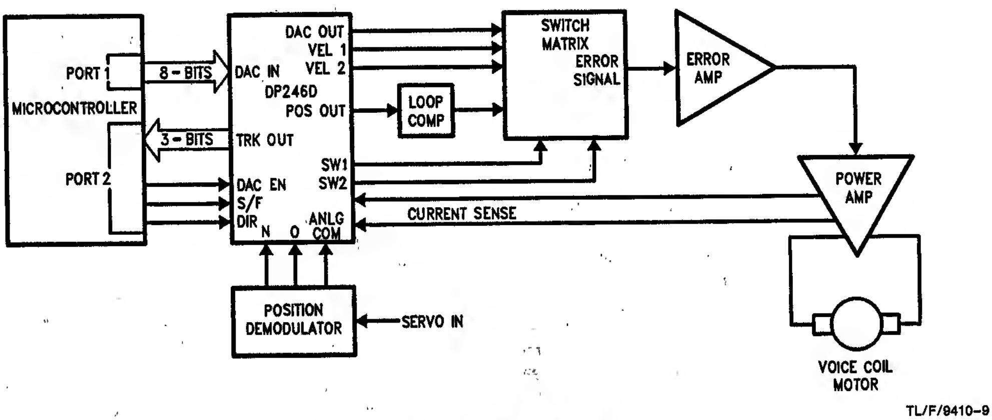


FIGURE 6. Typical Application Setup

National Semiconductor

2470A Servo Demodulator

General Description

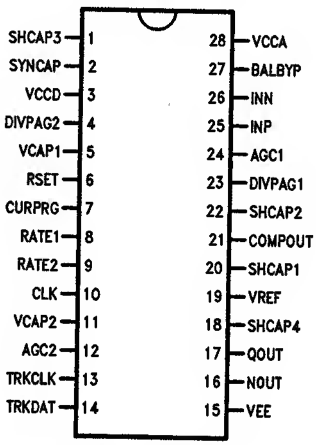
The new 2470A servo demodulator decodes the quadrature di-bit pattern from the dedicated servo surface providing position and data information.

Features

- Quadrature positions signals
- Phase locked to servo pattern with embedded lock indication
- Track data and track clock for data encoding
- AGC amplifier with 38 dB range
- Servo fields to 400 kHz
- Compatible with the 24H80 servo preamp and 2460 servo control chip
- Standard 5V and 12V supplies
- New phase detector eliminates jitter due to dropped sync's
- New lock detector uses sync pulse location to determine sync. Dropped pulses are not out of sync conditions.
- New ±20% VCO with extended frequency capability (>30 MHz)
- New totem pole TTL outputs
- New sync detector eliminates one shot multivibrator setting
- New sample and hold circuits eliminate output droop and glitching of the quadrature circuits
- New reference centers the quadrature outputs in the 12V supply
- New sync window controller prevents erroneous pulses from reaching the phase detector for a second level of jitter prevention

Connection Diagrams

28-Pin Molded DIP



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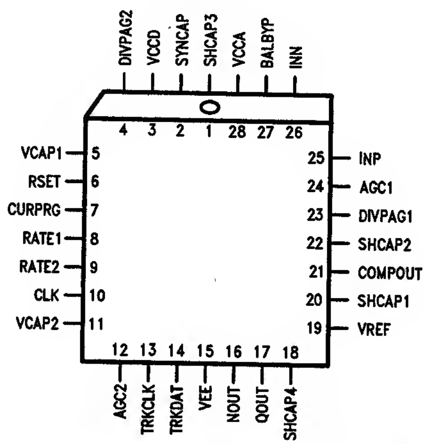
Top View
† Order Number 2470PC
‡ See NS Package Number N28B

28 PLCC



TL/F/9411-2

Top View
† Order Number 2470QC
‡ See NS Package Number V28A

† For most current order information, contact your local sales office.
‡ For most current package information, contact product marketing.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +175°C
Operating Temperature	0°C to +70°C
Lead Temperature Ceramic DIP (10 sec.)	300°C
Internal Power Dissipation	2.5W
Supply Voltage V_{CCD}	6V
Supply Voltage V_{CCA}	15V

2470A Electrical Specification T_A = 25°C, V_{CCD} = 5V, V_{VCCA} = 12V

Parameter	Conditions	Min	Typ	Max	Units
AGC AMPLIFIER					
Max Voltage Gain	Input Freq. = 1 MHz	40	46		dB
AGC Range	Input Freq. = 1 MHz	20	36		dB
Frequency Response			10		MHz
Input Voltage Range		30		300	mV
Output Voltage		3.0	3.3	3.6	V_{PP}
Common Mode Voltage			8.2		V
QUADRATURE OUTPUTS (Referred to 6V ref; R_L = 20k)					
Output Voltage	R_L = 20k	3.0	3.3	3.6	V_{PP}
Output Impedance				100	Ω
Output Offset Voltage			±5	+20	mV
Output Current	(Note: Out Impedance)		5	6	mA
VOLTAGE REFERENCE					
Output Voltage		5.88	6.00	6.12	V
Output Current			5	6	mA
V_{CO}					
Max Frequency V_{CO} (Ctr)			30		MHz
PLL System Performance using sine^3 Waveform as Servo Reference. Frame(center) = V_{CO}(center)/divider ratio.					
Acquisition Range		±10%	±15%		frame(ctr)
Dropped Sync Endurance		15	40	—	frames
Maximum Frame Rate		400			kHz
LOGIC					
Input Voltage Low				0.8	V
Input Voltage High		2.0			V
Output Voltage Low				0.5	V
Output Voltage High		2.7			V
Risetime	10%–90%		9	20	ns
Falltime	10%–90%		4	14	ns

DIVIDER TABLE Ratio = V_{CO} Frequency ÷ Frame Rate

DIVPAG1	DIVPAG2	RATIO
0	0	32
1	0	64
0	1	96
1	1	128

Power Supply Ratings

Parameter	Conditions	Min	Typ	Max	Units
V_{CCD} (5V)			80	100	mA
V_{CCA} (12V)			40	60	mA

Features of the 2470A Servo Demodulator

1) The sync detecting operation is based on the servo disk's own timing and eliminates the need to precisely set a resistor-capacitor time constant for the di-bit detecting one shot timer. The new circuit uses a single low precision capacitor.

2) The phase detector has a linear phase vs. output detection scheme as an improvement over the one shot scheme. The circuit performs no detection for dropped sync pulses and when in lock as defined by the lock detector, it will only detect in a predefined window. These features eliminate jitter caused by dropped pulses and/or bad servo areas on the disk. Also eliminated are the phase detector external components.

   Out of lock conditions require acquisition aids to achieve lock. Should a sync pulse show outside the sync window (2 of 32 counts in a servo field), aperature control circuits realign the sync pulse with the sync window by resetting the decoder and enlarge the next window to find a sync pulse with the VCO's ±20% tuning range. The limited range on the VCO prevents 2X locks. The aperature control prevents the dropped pulse ignoring phase detector from achieving non-integral false locks. The window realignment and enlargement is disabled during lock to prevent erroneous sync pulses from upsetting the decoder.

3) The new lock detector ignores dropped pulses in testing for in and out of lock conditions. Should a sync pulse appear the detector records whether or not it appeared in the normal sync window. The lock detector uses four consecutive sync pulses either all out or all in the sync window to determine lock status. The lock detector enables and disables the aperature control for the phase detector and the sync data detector.

4) The 2470A has a VCO with improved performance. It has > 30 MHz operation and a restricted tuning range of ±20%. Tuning circuits will reduce jitter due to parasitic couplings into the VCO.

5) New sample hold circuits for the N and Q decoders eliminate the droop in the N and Q outputs. The sample holds are opened immediately after the peak detection is complete. This eliminates droop induced offsets and glitching.

6) TTL totem pole outputs eliminates the need for resistive pullup for the output. Switching times of 10 ns are achieved.

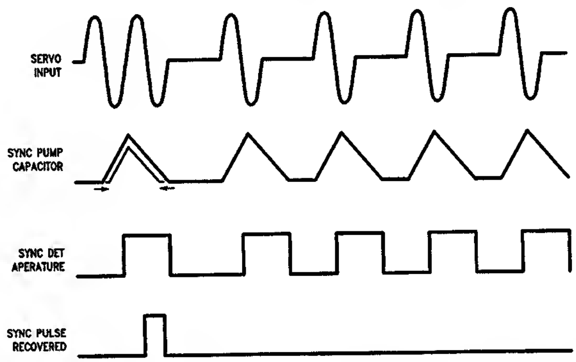
7) The analog reference is 6V. Centering in the 12V supply lines is easier. The 6V reference maintains compatibility with the 2460 servo controller and the 24H80 preamp.

List of Lead Functions

Lead	Name	Function
INPUT SIGNALS		
23 4	DIVPAG1 DIVPAG2	Programs the prescaler for the VCO Divide ratios are 32, 64, 96 and 128
7	CURPRG	Voltage sets PLL charge pump bias current
15	V_{EE}	Ground 0V
3	V_{CCD}	+5V supply
28	V_{CCA}	+12V supply
25 26	INP INN	Composite inputs to the AGC amplifier
OUTPUTS		
13	TRKCLK	Clock output for data during lock, TTL
14	TRKDAT	Data from dropped sync pulses TTL
10	CLK	VCO output TTL
21	COMPOUT	Output of AGC amplifier @8.2V CM
19	V_{REF}	6V reference for N and Q outputs
16	N_{OUT}	Normal position signal @6V CM
17	Q_{OUT}	Quadrature position signal @6V CM

List of Lead Functions (Continued)

Lead	Name	Function
EXTERNAL COMPONENTS		
2	SYNCAP	Timing capacitor for the sync detector
5–11	V_{CAP} 1 & 2	VCO timing capacitor
8–9	Rate 1 & 2	PLL loop filter
27	BALBYP	DC offset restore filter capacitor.
24	AGC1	AGC system loop filter
12	AGC2	AGC2 Pin includes an amplitude control function. This pin has a nominal voltage of 5V. The amplitude increases according to the formula: $\frac{V_{(COMPOUT\ P\text{-}P)} - V_{(COMPOUT\ NOM\ P\text{-}P)}}{V_{(AGC2)} - V_{(AGC2\ NOM)}} = -0.7$ AGC2 is Pin 12 and COMPOUT is Pin 21.
6	R_{SET}	Sets the VCO bias currents I < 2 mA
20, 22, 1, 18	SHCAP 1 . . . 4	Four sample hold capacitors



The sync pulse gate is triggered by the sync det aperature and is locked open until the sync goes to zero. The locking mechanism prevents clipping the negative edge of the sync.

FIGURE 1. Sync Detector Diagram

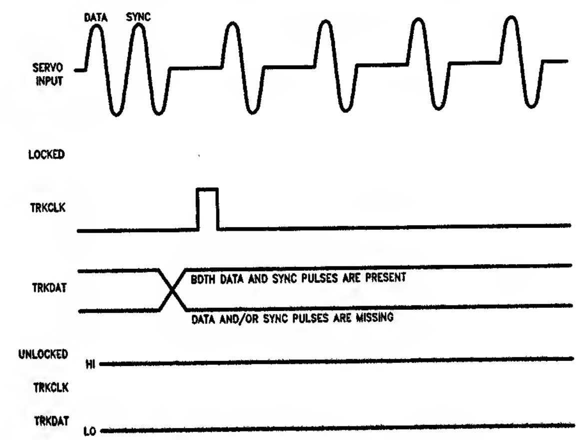


FIGURE 2. Track Data Output Information

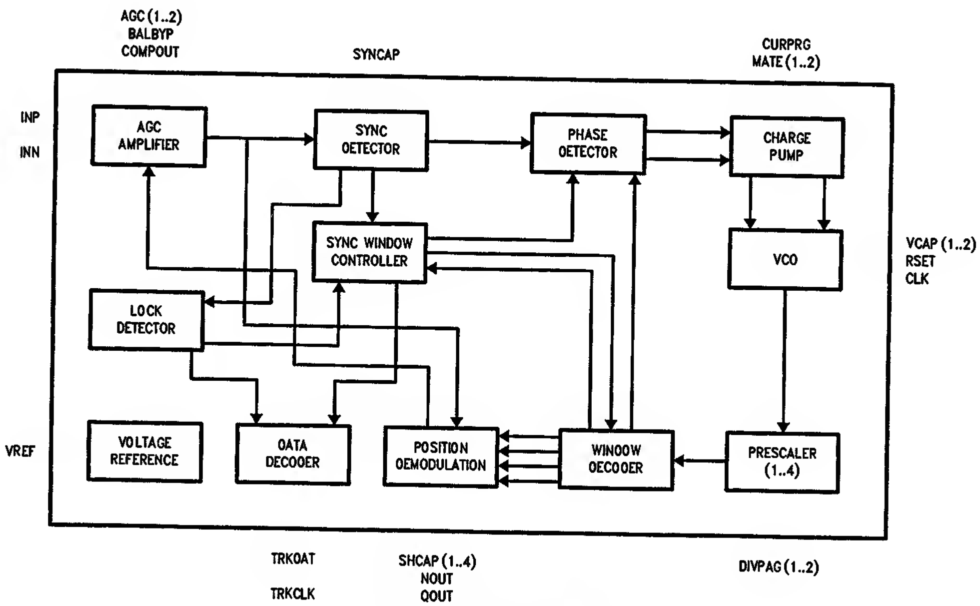


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FIGURE 3. 2470A Block Diagram

This test circuit runs at about a 136 kHz frame rate

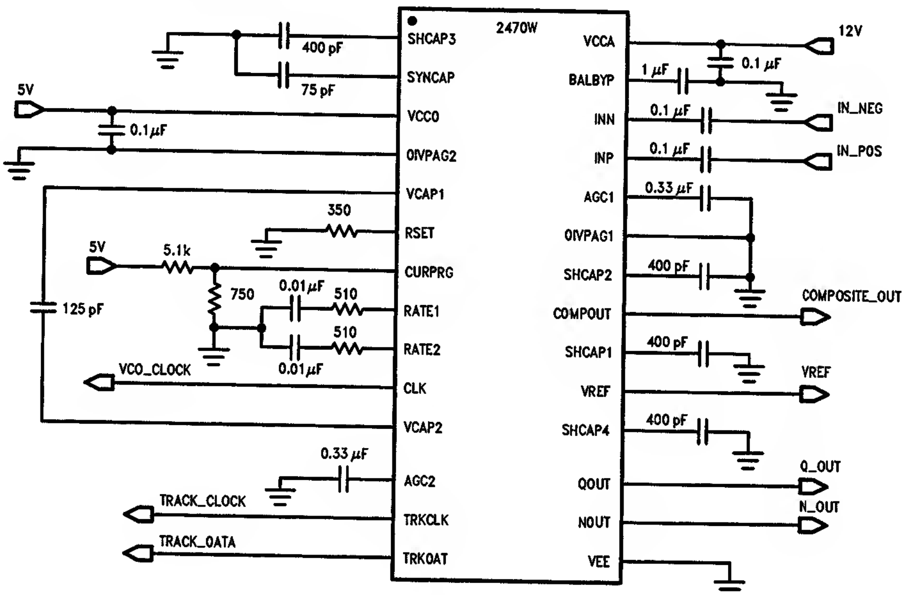

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FIGURE 4. 2470A Test Circuit